THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 12

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Ex parte JAYANTI L. GANDHI

Appeal No. 96-3051
Application 08/023,693[1]

ON BRIEF

Before HAIRSTON, JERRY SMITH and FLEMING, ***Administrative Patent Judges***.

FLEMING, ***Administrative Patent Judge***.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 1 through 12, all of the claims pending in the present application.

The invention relates to a method and apparatus for insuring the atomicity of atomic instructions. On page 5 of the specification, Appellant discloses an exemplary architecture of

[1] Application for patent filed February 26, 1993.

the invention as shown in Figure 2a. A first buffer 60 outputs a control bit which is visible to the user as a bit in a register, Register A. This bit is read and write accessible. The buffer 60 has write line input 65, read input 70, data in 80 and data out 85. Appellant discloses on pages 6 and 7 of the specification that output 85 of buffer 60 which provides the control bit is inputted to a second buffer 90. The second buffer 90 outputs a status bit visible at a user visible register which is read only. The status bit is updated when the control bit is supplied to the DIN input of the second buffer 90. The control bit is delayed a predetermined time by delay means 95 which is the amount of time required for an atomic instruction to be executed. The state of the status bit, although visible and readable by the user, is not controllable except through the setting of the control bit.

The independent claim 1 is reproduced as follows:

1. A system for executing atomic instructions comprising:

means for storing a plurality of instructions, comprising at least one atomic instruction;

processor means for executing instructions comprising;

means for setting and resetting a control bit in a visible register, which is read and write accessible by the user,

delay means coupled to the control bit for receiving the value of the control bit and delaying the output of the value of the control bit a predetermined amount of time,

means for setting and resetting a status bit which is read only accessible to a user in a visible register, said status bit coupled to the output of the delay means to receive the value of the control bit output by the delay means; and

control means for preventing subsequent instructions to be executed until the status bit is set to a first state;

wherein the atomic instruction competes execution within the predetermined amount of time and prior to execution of subsequent instructions.

The Examiner relies on the following references:

Boudreau	4,503,495	Mar. 5, 1985
Stumpf et al. (Stumpf)	5,175,829	Dec. 29, 1992

Sowell, Programming in Assembly Language, Macro-11, 1984, pages 174-177 and 313-327.

Claims 1, 2, 4 through 7, 11 and 12 stand rejected under 35 U.S.C. § 103 as being unpatentable over Stumpf and Boudreau.

Claims 3, 8, 9 and 10 stand rejected under 35 U.S.C. § 103 as being unpatentable over Stumpf, Boudreau and Sowell.

Rather than reiterate the arguments of Appellant and the Examiner, reference is made to the brief and answer for the respective details thereof.

OPINION

We will not sustain the rejection of claims 1 through 12 under 35 U.S.C. § 103.

The Examiner has failed to set forth a ***prima facie*** case of obviousness. It is the burden of the Examiner to establish why one having ordinary skill in the art would have been led to the claimed invention by the express teachings or suggestions found in the prior art, or by implications contained in such teachings or suggestions. ***In re Sernaker***, 702 F.2d 989, 995, 217 USPQ 1, 6 (Fed. Cir. 1983). "Additionally, when determining obviousness, the claimed invention should be considered as a whole; there is no legally recognizable 'heart' of the invention." ***Para-Ordnance Mfg. v. SGS Importers Int'l, Inc.***, 73 F.3d 1085, 1087, 37 USPQ2d 1237, 1239 (Fed. Cir. 1995), ***citing W. L. Gore & Assocs., Inc. v. Garlock, Inc.***, 721 F.2d 1540, 1548, 220 USPQ 303, 309 (Fed. Cir. 1983), ***cert. denied***, 469 U.S. 851 (1984).

Appellant argues on page 4 of the brief that Stumpf, Boudreau and Sowell, together or individually, fail to teach or suggest a visible register storing a control bit which is read and write accessible by the user as recited in Appellant's claims. We note that Appellant's claim 1 recites a "means for

setting and resetting a control bit in a visible register, which is read and write accessible by the user." We note that the other independent claim, claim 7, recites "a first buffer, the output of which is visible as a control bit in a register, said buffer being read and write accessible to a user." Finally, we note that the only other independent claim, claim 11, recites "setting a control bit in a visible register to a first state, said control bit being read and write accessible."

The Examiner agrees on page 4 of the answer that Stumpf does not explicitly teach a means for setting and resetting a control bit. The Examiner argues that Boudreau teaches a means for setting and resetting a control bit in Figure 2, item 405. The Examiner further argues on page 8 that Boudreau teaches a control bit in a user visible register in column 21, lines 7-13.

In column 4, lines 14-26, Boudreau discloses that his invention is concerned with a "method and apparatus for detecting use of a common resource, such as a bus, by a particular device connected to the common resource." Boudreau teaches that a device is granted use of the common resource based upon whether the device has the highest priority of the devices making the request. A common bus utilization detection logic, having no connection directly with the particular device of interest, is

connected to the common resource. The common bus utilization detection logic monitors the priority of the devices requesting use of the common resource and thereby monitors the devices that are granted access to the common resource. Boudreau states in column 4, lines 39-40, that Figure 2 "is a logic diagram of the common bus utilization detection logic" of his invention.

In column 54, line 41 through column 55, line 8, Boudreau teaches that the common bus utilization detection logic of Figure 2 monitors bus control network lines (BSREQT+ & BSDCNN+) and the nine priority network lines (BSAUOK+-BSIUOK+) of the common bus and sets CPU bus master flip-flop 402 (a binary ONE at CPDCNN+) when a lower priority device has become bus master and the information placed on the common bus by the lower priority device has become stable. The common bus utilization detection logic CPU resets the bus master flip-flop 402 (a binary ZERO at CPDCNN+) when the slave device responds.

In column 55, line 9 through column 56, line 48, Boudreau discloses the operation of the common bus utilization detection logic in further detail. Boudreau teaches in column 55, lines 51-58, that all nine priority signals (BSAUOK+-BSIUOK+) will be a binary ONE when a lower priority device has become bus master. This causes the NAND gate 401 to output a binary ZERO and set CPU

DCN flip-flop 405 (CPDCND+ is a binary ONE). The output of CPU DCN flip-flop 405 is supplied to the data (D) input to the CPU master flip-flop 402.

In column 55, line 59 through column 56, line 9, Boudreau discloses the CPU DCN flip-flop 405 is clocked sixty nanoseconds after the bus data cycle begins. The bus data cycle begins when BSDCNN+ becomes a binary ONE. The delay is provided by delay means 404 and the purpose of the delay is to insure that the information presented on the common bus has stabilized.

In column 56, lines 10-23, Boudreau discloses that the CPU bus master flip-flop 402 remains set until the responding slave unit on the common bus responds by setting to binary ONE the acknowledgments signal (BSACKR+), the negative acknowledge signal (BSNAKR+) or the wait signal (BSwait+). This resets the CPU DNC flip-flop 405 and CPU master flip-flop 402. In column 56, lines 34-40, Boudreau teaches that the only purpose of the CPU DNC flip-flop 405 is to assure that the output of the NAND gate 401 is preserved until the expiration of the 60 nanosecond delay and does not disappear before the CPU bus master flip-flop 402 is clocked.

We find that the Examiner erred by finding that Boudreau's CPU DNC flip-flop 405 meets a means for setting and resetting a

control bit in a visible register, which is read and write accessible by the user as claimed by Appellant. Boudreau does not teach that the CPU DNC flip-flop 405 is read or write accessible by the user. Boudreau teaches that the only purpose of CPU DNC flip-flop 405 is to provide the proper timing of internal signals within a bus arbitration monitor and is not read or write accessible by the user. Thus, Boudreau fails to teach or suggest a means for setting and resetting a control bit in a visible register, which is read and write accessible by the user as claimed by Appellant.

On page 6 of the brief, Appellant argues that Stumpf, Boudreau and Sowell, together or individually, fail to teach or suggest preventing subsequent instructions until the atomic instructions completes execution by delaying subsequent instructions by a predetermined amount of time equal to amount of time to execute an atomic instruction. We note that Appellant's claim 1 recites a delay means coupled between the output of the first buffer and the input to the second buffer, such that the state of the status bit equals the state of the control bit after the delay; a "control means for preventing subsequent instructions to be executed until the status bit is set to a first state, wherein the atomic instruction completes execution within the

predetermined amount of time and prior to execution of subsequent instructions." We note that Appellant's Claim 7 recites "a control means for preventing execution of instructions subsequent to the atomic instruction until execution of the atomic instruction is complete." Finally, we note that the only remaining independent claim, claim 11, recites "when an atomic instruction is to be executed, ... coupling the control bit to a status bit ... through a delay means having a predetermined delay such that the status bit is updated with the value of the control bit after the predetermined delay ... preventing execution of subsequent instructions until the status bit is set to the first state."

On page 4 of the answer, the Examiner agrees that Stumpf fails to teach a delay means. The Examiner argues that Boudreau teaches a delay means in Figure 2, item 402. The Examiner argues that it would have been obvious to modify Stumpf to use the Boudreau common bus utilization detection logic of Figure 2 to control atomic operations. However, the Examiner did not address the issue of the Appellant's claim limitations requiring a delay of time to execute an atomic instruction.

As shown above, Boudreau teaches that the delay for updating the CPU Bus Master flip-flop 402 is the time required for the

information on the bus to stabilize. Boudreau does not teach or suggest delaying executing subsequent instructions based upon execution time. We agree that Stumpf teaches a plurality of processors sharing a common memory and a common bus wherein the processor performing an atomic operation prevents memory access interruptions by other processors by locking out other processors during the atomic operation. However, Stumpf does not teach a control means for preventing subsequent instructions to be executed for a predetermined amount of time required to execute an atomic instruction.

Stumpf teaches that the processor which has access to the common bus may not be interrupted when the processor is performing an atomic operation. In column 2, lines 13-68, Stumpf teaches that the processor which is to perform the atomic operation initiates a memory lock by executing a memory load lock instruction. Stumpf does not teach that the subsequent instructions which are executed by the processor that has access to the common bus are prevented from being executed for a predetermined amount of time required to execute an atomic instruction.

Stumpf further teaches that the processor that initiates the lock must also remove the lock. In column 3, lines 50-64,

Stumpf teaches that a lock timeout is to be used to ward against system deadlock resulting from a processor failure to remove the lock. Stumpf does not teach that the time period is sufficient for the execution time of an atomic instruction, but instead only teaches that the time period be large compared to the expected lock holding duration. Stumpf teaches that the processor which has access to the common bus is programmed by executing a lock release instruction to remove the lock. Therefore, Stumpf fails to teach a control means for preventing subsequent instructions to be executed until the status bit is set to a first state wherein the atomic instruction completes execution within the predetermined amount of time and prior to execution of subsequent instructions.

The Federal Circuit states that "[t]he mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." ***In re Fritch***, 972 F.2d 1260, 1266 n.14, 23 USPQ2d 1780, 1783-84 n.14 (Fed. Cir. 1992), ***citing In re Gordon***, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984). "Obviousness may not be established using hindsight or in view of the teachings or suggestions of the inventor." ***Para-Ordnance Mfg. v. SGS Importers Int'l***, 73 F.3d at

1087, 37 USPQ2d at 1239, ***citing W. L. Gore & Assocs., Inc. v. Garlock, Inc.***, 721 F.2d at 1551, 1553, 220 USPQ at 311, 312-13.

Upon reviewing Boudreau, Stumpf and Sowell, we fail to find any suggested desirability of modifying Boudreau to obtain a system or method for executing atomic instructions as recited in Appellant's claims 1 through 12.

We have not sustained the rejection of claims 1 through 12 under 35 U.S.C. § 103. Accordingly, the Examiner's decision is reversed.

REVERSED

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